Intel Xeon Phi Processor High Performance Programming Knights Landing Edition

BPF and related observability tools give software professionals unprecedented visibility into software, helping them analyze operating system and application performance, troubleshoot code, and strengthen security. BPF Performance Tools: Linux System and Application Observability is the industry's most comprehensive guide to using these tools for observability. Brendan Gregg, author of the industry's definitive guide to system performance, introduces powerful new methods and tools for doing analysis that leads to more robust, reliable, and safer code. This authoritative guide: Explores a wide spectrum of software and hardware targets Thoroughly covers open source BPF tools from the Linux Foundation iovisor project's bcc and bpftrace repositories Summarizes performance engineering and kernel internals you need to understand Provides and discusses 150+ bpftrace tools, including 80 written specifically for this book: tools you can run as-is, without programming — or customize and develop further, using diverse interfaces and the bpftrace front-end You'll learn how to use BPF (eBPF) tracing tools to analyze CPUs, memory, disks, file systems, networking, languages, applications, containers, hypervisors, security, and the Linux kernel. You'll move from basic to advanced tools and techniques, producing new metrics, stack traces, custom latency histograms, and more. It's like having a superpower: with Gregg's guidance and tools, you can analyze virtually everything that impacts system performance, so you can improve virtually any Linux operating system or application.
This book is an all-in-one source of information for programming the Second-Generation Intel Xeon Phi product family also called Knights Landing. The authors provide detailed and timely Knights Landingspecific details, programming advice, and real-world examples. The authors distill their years of Xeon Phi programming experience coupled with insights from many expert customers — Intel Field Engineers, Application Engineers, and Technical Consulting Engineers — to create this authoritative book on the essentials of programming for Intel Xeon Phi products. Intel® Xeon PhiTM Processor High-Performance Programming is useful even before you ever program a system with an Intel Xeon Phi processor. To help ensure that your applications run at maximum efficiency, the authors emphasize key techniques for programming any modern parallel computing system whether based on Intel Xeon processors, Intel Xeon Phi processors, or other high-performance microprocessors. Applying these techniques will generally increase your program performance on any system and prepare you better for Intel Xeon Phi processors. A practical guide to the essentials for programming Intel Xeon Phi processors Definitive coverage of the Knights Landing architecture Presents best practices for portable, high-performance computing and a familiar and proven threads and vectors programming model Includes real world code examples that highlight usages of the unique aspects of this new highly parallel and high-performance computational product Covers use of MCDRAM, AVX-512, Intel® Omni-Path fabric, many-cores (up to 72), and many threads (4 per core) Covers software developer tools, libraries and programming models Covers using Knights Landing as a processor and a coprocessor
This book constitutes revised selected papers from 7 workshops that were held in conjunction with the ISC High Performance 2016 conference in Frankfurt, Germany, in

June 2016. The 45 papers presented in this volume were carefully reviewed and selected for inclusion in this book. They stem from the following workshops: Workshop on Exascale Multi/Many Core Computing Systems, E-MuCoCoS; Second International Workshop on Communication Architectures at Extreme Scale, ExaComm; HPC I/O in the Data Center Workshop, HPC-IODC; International Workshop on OpenPOWER for HPC, IWOPH; Workshop on the Application Performance on Intel Xeon Phi – Being Prepared for KNL and Beyond, IXPUG; Workshop on Performance and Scalability of Storage Systems, WOPSSS; and International Workshop on Performance Portable Programming Models for Accelerators, P3MA.

Programming has become a significant part of connecting theoretical development and scientific application computation. Fluid dynamics provide an important asset in experimentation and theoretical analysis. Analysis and Applications of Lattice Boltzmann Simulations provides emerging research on the efficient and standard implementations of simulation methods on current and upcoming parallel architectures. While highlighting topics such as hardware accelerators, numerical analysis, and sparse geometries, this publication explores the techniques of specific simulators as well as the multiple extensions and various uses. This book is a vital resource for engineers, professionals, researchers, academics, and students seeking current research on computational fluid dynamics, high-performance computing, and numerical and flow simulations.

Intel® Xeon PhiTM Coprocessor Architecture and Tools: The Guide for Application Developers provides developers a comprehensive introduction and in-depth look at the Intel Xeon Phi coprocessor architecture and the corresponding parallel data structure tools and algorithms used in the various technical computing applications for which it is suitable. It also examines the source code-level optimizations that can be performed to exploit the powerful features of the processor. Xeon Phi is at the heart of world's fastest commercial supercomputer, which thanks to the massively parallel computing capabilities of Intel Xeon Phi processors coupled with Xeon Phi coprocessors attained 33.86 teraflops of benchmark performance in 2013. Extracting such stellar performance in real-world applications requires a sophisticated understanding of the complex interaction among hardware components, Xeon Phi cores, and the applications running on them. In this book, Rezaur Rahman, an Intel leader in the development of the Xeon Phi coprocessor and the optimization of its applications, presents and details all the features of Xeon Phi core design that are relevant to the practice of application developers, such as its vector units, hardware multithreading, cache hierarchy, and host-to-coprocessor communication channels. Building on this foundation, he shows developers how to solve real-world technical computing problems by selecting, deploying, and optimizing the available algorithms and data structure alternatives matching Xeon Phi's hardware characteristics. From Rahman's practical descriptions and extensive code examples, the reader will gain a working knowledge of the Xeon Phi vector instruction set and the Xeon Phi microarchitecture whereby cores execute 512-bit instruction streams in parallel.

High Performance Parallelism Pearls Volume 2 offers another set of examples that demonstrate how to leverage parallelism. Similar to Volume 1, the techniques included here explain how to use processors and coprocessors with the same programming – illustrating the most effective ways to combine Xeon Phi coprocessors with Xeon and

other multicore processors. The book includes examples of successful programming efforts, drawn from across industries and domains such as biomed, genetics, finance, manufacturing, imaging, and more. Each chapter in this edited work includes detailed explanations of the programming techniques used, while showing high performance results on both Intel Xeon Phi coprocessors and multicore processors. Learn from dozens of new examples and case studies illustrating "success stories" demonstrating not just the features of Xeon-powered systems, but also how to leverage parallelism across these heterogeneous systems. Promotes write-once, run-anywhere coding, showing how to code for high performance on multicore processors and Xeon Phi Examples from multiple vertical domains illustrating real-world use of Xeon Phi coprocessors Source code available for download to facilitate further exploration The year 2019 marked four decades of cluster computing, a history that began in 1979 when the first cluster systems using Components Off The Shelf (COTS) became operational. This achievement resulted in a rapidly growing interest in affordable parallel computing for solving compute intensive and large scale problems. It also directly lead to the founding of the Parco conference series. Starting in 1983, the International Conference on Parallel Computing, ParCo, has long been a leading venue for discussions of important developments, applications, and future trends in cluster computing, parallel computing, and high-performance computing. ParCo2019, held in Prague, Czech Republic, from 10 – 13 September 2019, was no exception. Its papers, invited talks, and specialized mini-symposia addressed cutting-edge topics in computer architectures, programming methods for specialized devices such as field programmable gate arrays (FPGAs) and graphical processing units (GPUs), innovative applications of parallel computers, approaches to reproducibility in parallel computations, and other relevant areas. This book presents the proceedings of ParCo2019, with the goal of making the many fascinating topics discussed at the meeting accessible to a broader audience. The proceedings contains 57 contributions in total, all of which have been peer-reviewed after their presentation. These papers give a wide ranging overview of the current status of research, developments, and applications in parallel computing. Programming is now parallel programming. Much as structured programming revolutionized traditional serial programming decades ago, a new kind of structured programming, based on patterns, is relevant to parallel programming today. Parallel computing experts and industry insiders Michael McCool, Arch Robison, and James Reinders describe how to design and implement maintainable and efficient parallel algorithms using a pattern-based approach. They present both theory and practice, and give detailed concrete examples using multiple programming models. Examples are primarily given using two of the most popular and cutting edge programming models for parallel programming: Threading Building Blocks, and Cilk Plus. These architecture-independent models enable easy integration into existing applications, preserve investments in existing code, and speed the development of parallel applications. Examples from realistic contexts illustrate patterns and themes in parallel algorithm design that are widely applicable regardless of implementation technology. The patterns-based approach offers structure and insight that developers can apply to a variety of parallel programming models Develops a composable, structured, scalable, and machine-independent approach to parallel computing Includes detailed examples

in both Cilk Plus and the latest Threading Building Blocks, which support a wide variety
of computers

The most powerful computers work by harnessing the combined computational
power of millions of processors, and exploiting the full potential of such large-
scale systems is something which becomes more difficult with each succeeding
generation of parallel computers. Alternative architectures and computer
paradigms are increasingly being investigated in an attempt to address these
difficulties. Added to this, the pervasive presence of heterogeneous and parallel
devices in consumer products such as mobile phones, tablets, personal
computers and servers also demands efficient programming environments and
applications aimed at small-scale parallel systems as opposed to large-scale
supercomputers. This book presents a selection of papers presented at the
conference: Parallel Computing (ParCo2017), held in Bologna, Italy, on 12 to 15
September 2017. The conference included contributions about alternative
approaches to achieving High Performance Computing (HPC) to potentially
surpass exa- and zetascale performances, as well as papers on the application
of quantum computers and FPGA processors. These developments are aimed at
making available systems better capable of solving intensive computational
scientific/engineering problems such as climate models, security applications and
classic NP-problems, some of which cannot currently be managed by even the
most powerful supercomputers available. New areas of application, such as
robotics, AI and learning systems, data science, the Internet of Things (IoT), and
in-car systems and autonomous vehicles were also covered. As always,
ParCo2017 attracted a large number of notable contributions covering present
and future developments in parallel computing, and the book will be of interest to
all those working in the field.

This book constitutes the refereed proceedings papers from the 8th International
Workshop on Performance Modeling, Benchmarking and Simulation of High
Performance Computing Systems, PMBS 2017, held in Denver, Colorado, USA,
in November 2017. The 10 full papers and 3 short papers included in this volume
were carefully reviewed and selected from 36 submissions. They were organized
in topical sections named: performance evaluation and analysis; performance
modeling and simulation; and short papers.

This book constitutes revised selected papers from the 26th Argentine Congress
on Computer Science, CACIC 2020, held in San Justo, Buenos Aires, Argentina
in October 2020. Due to the COVID-19 pandemic the conference was held in a
virtual mode. The 21 full papers and 3 short papers presented in this volume
were carefully reviewed and selected from a total of 118 submissions. They were
organized in topical sections named: intelligent agents and systems; distributed
and parallel processing; computer technology applied to education; graphic
computation, images and visualization; software engineering; databases and
data mining; hardware architectures, networks, and operating systems;
innovation in software systems; signal processing and real-time systems;

innovation in computer science education; computer security; and digital governance and smart cities.

This book constitutes the refereed proceedings of the 8th International Symposium on Parallel Architecture, Algorithm and Programming, PAAP 2017, held in Haikou, China, in June 2017. The 50 revised full papers and 7 revised short papers presented were carefully reviewed and selected from 192 submissions. The papers deal with research results and development activities in all aspects of parallel architectures, algorithms and programming techniques.

In view of the growing presence and popularity of multicore and manycore processors, accelerators, and coprocessors, as well as clusters using such computing devices, the development of efficient parallel applications has become a key challenge to be able to exploit the performance of such systems. This book covers the scope of parallel programming for modern high performance computing systems. It first discusses selected and popular state-of-the-art computing devices and systems available today, These include multicore CPUs, manycore (co)processors, such as Intel Xeon Phi, accelerators, such as GPUs, and clusters, as well as programming models supported on these platforms. It next introduces parallelization through important programming paradigms, such as master-slave, geometric Single Program Multiple Data (SPMD) and divide-and-conquer. The practical and useful elements of the most popular and important APIs for programming parallel HPC systems are discussed, including MPI, OpenMP, Pthreads, CUDA, OpenCL, and OpenACC. It also demonstrates, through selected code listings, how selected APIs can be used to implement important programming paradigms. Furthermore, it shows how the codes can be compiled and executed in a Linux environment. The book also presents hybrid codes that integrate selected APIs for potentially multi-level parallelization and utilization of heterogeneous resources, and it shows how to use modern elements of these APIs. Selected optimization techniques are also included, such as overlapping communication and computations implemented using various APIs. Features: Discusses the popular and currently available computing devices and cluster systems Includes typical paradigms used in parallel programs Explores popular APIs for programming parallel applications Provides code templates that can be used for implementation of paradigms Provides hybrid code examples allowing multi-level parallelization Covers the optimization of parallel programs

The six-volume set LNCS 10404-10409 constitutes the refereed proceedings of the 17th International Conference on Computational Science and Its Applications, ICCSA 2017, held in Trieste, Italy, in July 2017. The 313 full papers and 12 short papers included in the 6-volume proceedings set were carefully reviewed and selected from 1052 submissions. Apart from the general tracks, ICCSA 2017 included 43 international workshops in various areas of computational sciences, ranging from computational science technologies to specific areas of computational sciences, such as computer graphics and virtual reality.

Furthermore, this year ICCSA 2017 hosted the XIV International Workshop On Quantum Reactive Scattering. The program also featured 3 keynote speeches and 4 tutorials.

Contemporary High Performance Computing: From Petascale toward Exascale, Volume 3 focuses on the ecosystems surrounding the world's leading centers for high performance computing (HPC). It covers many of the important factors involved in each ecosystem: computer architectures, software, applications, facilities, and sponsors. This third volume will be a continuation of the two previous volumes, and will include other HPC ecosystems using the same chapter outline: description of a flagship system, major application workloads, facilities, and sponsors. Features: Describes many prominent, international systems in HPC from 2015 through 2017 including each system's hardware and software architecture Covers facilities for each system including power and cooling Presents application workloads for each site Discusses historic and projected trends in technology and applications Includes contributions from leading experts Designed for researchers and students in high performance computing, computational science, and related areas, this book provides a valuable guide to the state-of-the art research, trends, and resources in the world of HPC.

Parallel Programming with OpenACC is a modern, practical guide to implementing dependable computing systems. The book explains how anyone can use OpenACC to quickly ramp-up application performance using high-level code directives called pragmas. The OpenACC directive-based programming model is designed to provide a simple, yet powerful, approach to accelerators without significant programming effort. Author Rob Farber, working with a team of expert contributors, demonstrates how to turn existing applications into portable GPU accelerated programs that demonstrate immediate speedups. The book also helps users get the most from the latest NVIDIA and AMD GPU plus multicore CPU architectures (and soon for Intel® Xeon PhiTM as well). Downloadable example codes provide hands-on OpenACC experience for common problems in scientific, commercial, big-data, and real-time systems. Topics include writing reusable code, asynchronous capabilities, using libraries, multicore clusters, and much more. Each chapter explains how a specific aspect of OpenACC technology fits, how it works, and the pitfalls to avoid. Throughout, the book demonstrates how the use of simple working examples that can be adapted to solve application needs. Presents the simplest way to leverage GPUs to achieve application speedups Shows how OpenACC works, including working examples that can be adapted for application needs Allows readers to download source code and slides from the book's companion web page

This book explores energy efficiency techniques for high-performance computing (HPC) systems using power-management methods. Adopting a step-by-step approach, it describes power-management flows, algorithms and mechanism that are employed in modern processors such as Intel Sandy Bridge, Haswell, Skylake and other

architectures (e.g. ARM). Further, it includes practical examples and recent studies demonstrating how modem processors dynamically manage wide power ranges, from a few milliwatts in the lowest idle power state, to tens of watts in turbo state. Moreover, the book explains how thermal and power deliveries are managed in the context this huge power range. The book also discusses the different metrics for energy efficiency, presents several methods and applications of the power and energy estimation, and shows how by using innovative power estimation methods and new algorithms modern processors are able to optimize metrics such as power, energy, and performance. Different power estimation tools are presented, including tools that break down the power consumption of modern processors at sub-processor core/thread granularity. The book also investigates software, firmware and hardware coordination methods of reducing power consumption, for example a compiler-assisted power management method to overcome power excursions. Lastly, it examines firmware algorithms for dynamic cache resizing and dynamic voltage and frequency scaling (DVFS) for memory sub-systems.

Current high-performance computing clusters feature CPUs with 8 to 16 cores. The many-integrated-core (MIC) Intel Xeon Phi processors feature 60 or more cores on a single chip, with lower power consumption per core than CPUs. The Intel Xeon Phi Knights Landing (KNL) is the second-generation Xeon Phi processor released in 2016. It represents a significant improvement over the first-generation Knights Corner (KNC), since the KNL can serve as a standalone processor and has a 2D mesh interconnect on the chip to connect the cores to the 16 GB of high-performance memory on the chip. This architecture is very accessible to researchers who need only add a compiler flag to their code as a result of the x86 compatibility of each Xeon Phi core. But the different configurations available for the KNL add a layer of decisions for researchers on how to run their code. We use the Stampede cluster at the Texas Advanced Computing Center (TACC) for all hardware choices, since it is accessible to many researchers via an Extreme Science and Engineering Discovery Environment (XSEDE) allocation.

This book presents the latest findings in the areas of data management and smart computing, big data management, artificial intelligence and data analytics, along with advances in network technologies. It addresses state-of-the-art topics and discusses challenges and solutions for future development. Gathering original, unpublished contributions by scientists from around the globe, the book is mainly intended for a professional audience of researchers and practitioners in academia and industry.

This book constitutes revised selected papers from 10 workshops that were held as the ISC High Performance 2017 conference in Frankfurt, Germany, in June 2017. The 59 papers presented in this volume were carefully reviewed and selected for inclusion in this book. They stem from the following workshops: Workshop on Virtualization in High-Performance Cloud Computing (VHPC) Visualization at Scale: Deployment Case Studies and Experience Reports International Workshop on Performance Portable Programming Models for Accelerators (P^3MA) OpenPOWER for HPC (IWOPH) International Workshop on Data Reduction for Big Scientific Data (DRBSD) International Workshop on Communication Architectures for HPC, Big Data, Deep Learning and Clouds at Extreme Scale Workshop on HPC Computing in a Post Moore's Law World (HCPM) HPC I/O in the Data Center (HPC-IODC) Workshop on Performance and Scalability of Storage Systems (WOPSSS) IXPUG: Experiences on

Intel Knights Landing at the One Year Mark International Workshop on Communication Architectures for HPC, Big Data, Deep Learning and Clouds at Extreme Scale (ExaComm)

Book explains how to maximize the benefits of Intel's new dual-core and multi-core processors through a portable C++ library that works on Windows, Linux, Macintosh, and Unix systems.

Many-core parallel computing has now become very essential in high performance applications. With parallel processing now taking the main stage of direction in which to increase computing power we see the beginning of lighter core based many core processors. With NVIDIA's GPGPU being one of the initiators in this field we now have Intel's Many Integrated Core (MIC) architecture based processors in this field. In this paper we compare the performance of Intel's Xeon Phi with a Xeon CPU using a multi-threaded high memory application; Burrows-Wheeler Aligner. In this comparison we have essentially compared the newer generation of many core processors with the traditional multi-core server processor. The Intel Xeon Phi uses multiple x-86 based CPUs with wide vector processing unit while the Intel Xeon is Intel's sandy-bridge based high performance multi-core server CPU. Our results indicate that while the Intel Xeon Phi is able to process the application almost comparable to the Intel Xeon it still lacks a good efficient memory access compared to Intel Xeon which causes its overall performance to slow down when compared to Intel Xeon.

Authors Jim Jeffers and James Reinders spent two years helping educate customers about the prototype and pre-production hardware before Intel introduced the first Intel Xeon Phi coprocessor. They have distilled their own experiences coupled with insights from many expert customers, Intel Field Engineers, Application Engineers and Technical Consulting Engineers, to create this authoritative first book on the essentials of programming for this new architecture and these new products. This book is useful even before you ever touch a system with an Intel Xeon Phi coprocessor. To ensure that your applications run at maximum efficiency, the authors emphasize key techniques for programming any modern parallel computing system whether based on Intel Xeon processors, Intel Xeon Phi coprocessors, or other high performance microprocessors. Applying these techniques will generally increase your program performance on any system, and better prepare you for Intel Xeon Phi coprocessors and the Intel MIC architecture. A practical guide to the essentials of the Intel Xeon Phi coprocessor Presents best practices for portable, high-performance computing and a familiar and proven threaded, scalar-vector programming model Includes simple but informative code examples that explain the unique aspects of this new highly parallel and high performance computational product Covers wide vectors, many cores, many threads and high bandwidth cache/memory architecture.

This book constitutes the proceedings of the Second Latin American Conference on High Performance Computing, CARLA 2015, a joint conference of the High-Performance Computing Latin America Community, HPCLATAM, and the Conferencia Latino Americana de Computación de Alto Rendimiento, CLCAR, held in Petrópolis, Brazil, in August 2015. The 11 papers presented in this volume were carefully reviewed and selected from 17 submissions. They were organized in topical sections named: grid and cloud computing; GPU & MIC Computing: methods, libraries and applications; and scientific computing applications.

This book constitutes the refereed workshop proceedings of the 16th International Conference on Algorithms and Architectures for Parallel Processing, ICA3PP 2016, held in Granada, Spain, in December 2016. The 30 full papers presented were carefully reviewed and selected from 58 submissions. They cover many dimensions of parallel algorithms and architectures, encompassing fundamental theoretical approaches, practical experimental projects, and commercial components and systems trying to push beyond the limits of existing technologies, including experimental efforts, innovative systems, and investigations that identify weaknesses in existing parallel processing technology.

Written by high performance computing (HPC) experts, Introduction to High Performance Computing for Scientists and Engineers provides a solid introduction to current mainstream computer architecture, dominant parallel programming models, and useful optimization strategies for scientific HPC. From working in a scientific computing center, the author

This book constitutes revised selected papers from the 25th Argentine Congress on Computer Science, CACIC 2019, held in Río Cuarto, Argentina, in October 2019. The 27 full papers presented in this volume were carefully reviewed and selected from a total of 185 submissions. They were organized in topical sections named: intelligent agents and systems; distributed and parallel processing; computer technology applied to education; graphic computation, images and visualization; software engineering; databases and data mining; hardware architectures, networks, and operating systems; innovation in software systems; signal processing and real-time systems; computer security; innovation in computer science education; and digital governance and smart cities.

High Performance Parallelism Pearls shows how to leverage parallelism on processors and coprocessors with the same programming - illustrating the most effective ways to better tap the computational potential of systems with Intel Xeon Phi coprocessors and Intel Xeon processors or other multicore processors. The book includes examples of successful programming efforts, drawn from across industries and domains such as chemistry, engineering, and environmental science. Each chapter in this edited work includes detailed explanations of the programming techniques used, while showing high performance results on both Intel Xeon Phi coprocessors and multicore processors. Learn from dozens of new examples and case studies illustrating "success stories" demonstrating not just the features of these powerful systems, but also how to leverage parallelism across these heterogeneous systems. Promotes consistent standards-based programming, showing in detail how to code for high performance on multicore processors and Intel® Xeon PhiT Examples from multiple vertical domains illustrating parallel optimizations to modernize real-world codes Source code available for download to facilitate further exploration

This book constitutes the thoroughly refereed post-conference proceedings of the Third International Conference on High Performance Computing in Science and Engineering, HPCSE 2017, held in Karolinka, Czech Republic, in May 2017. The 15 papers presented in this volume were carefully reviewed and selected from 20 submissions. The conference provides an international forum for exchanging ideas among researchers involved in scientific and parallel computing, including theory and applications, as well as applied and computational mathematics. The focus of HPCSE

2017 was on models, algorithms, and software tools which facilitate efficient and convenient utilization of modern parallel and distributed computing architectures, as well as on large-scale applications.

The five-volume set LNCS 11536, 11537, 11538, 11539, and 11540 constitutes the proceedings of the 19th International Conference on Computational Science, ICCS 2019, held in Faro, Portugal, in June 2019. The total of 65 full papers and 168 workshop papers presented in this book set were carefully reviewed and selected from 573 submissions (228 submissions to the main track and 345 submissions to the workshops). The papers were organized in topical sections named: Part I: ICCS Main Track Part II: ICCS Main Track; Track of Advances in High-Performance Computational Earth Sciences: Applications and Frameworks; Track of Agent-Based Simulations, Adaptive Algorithms and Solvers; Track of Applications of Matrix Methods in Artificial Intelligence and Machine Learning; Track of Architecture, Languages, Compilation and Hardware Support for Emerging and Heterogeneous Systems Part III: Track of Biomedical and Bioinformatics Challenges for Computer Science; Track of Classifier Learning from Difficult Data; Track of Computational Finance and Business Intelligence; Track of Computational Optimization, Modelling and Simulation; Track of Computational Science in IoT and Smart Systems Part IV: Track of Data-Driven Computational Sciences; Track of Machine Learning and Data Assimilation for Dynamical Systems; Track of Marine Computing in the Interconnected World for the Benefit of the Society; Track of Multiscale Modelling and Simulation; Track of Simulations of Flow and Transport: Modeling, Algorithms and Computation Part V: Track of Smart Systems: Computer Vision, Sensor Networks and Machine Learning; Track of Solving Problems with Uncertainties; Track of Teaching Computational Science; Poster Track ICCS 2019 Chapter "Comparing Domain-decomposition Methods for the Parallelization of Distributed Land Surface Models" is available open access under a Creative Commons Attribution 4.0 International License via link.springer.com.

High Performance Parallelism Pearls shows how to leverage parallelism on processors and coprocessors with the same programming – illustrating the most effective ways to better tap the computational potential of systems with Intel Xeon Phi coprocessors and Intel Xeon processors or other multicore processors. The book includes examples of successful programming efforts, drawn from across industries and domains such as chemistry, engineering, and environmental science. Each chapter in this edited work includes detailed explanations of the programming techniques used, while showing high performance results on both Intel Xeon Phi coprocessors and multicore processors. Learn from dozens of new examples and case studies illustrating "success stories" demonstrating not just the features of these powerful systems, but also how to leverage parallelism across these heterogeneous systems. Promotes consistent standards-based programming, showing in detail how to code for high performance on multicore processors and Intel® Xeon PhiTM Examples from multiple vertical domains illustrating parallel optimizations to modernize real-world codes Source code available for download to facilitate further exploration

This book is an all-in-one source of information for programming the Second-Generation Intel Xeon Phi product family also called Knights Landing. The authors provide detailed and timely Knights Landingspecific details, programming advice, and real-world examples. The authors distill their years of Xeon Phi programming

experience coupled with insights from many expert customers Intel Field Engineers, Application Engineers, and Technical Consulting Engineers to create this authoritative book on the essentials of programming for Intel Xeon Phi products. "Intel(r) Xeon Phi Processor High-Performance Programming" is useful even before you ever program a system with an Intel Xeon Phi processor. To help ensure that your applications run at maximum efficiency, the authors emphasize key techniques for programming any modern parallel computing system whether based on Intel Xeon processors, Intel Xeon Phi processors, or other high-performance microprocessors. Applying these techniques will generally increase your program performance on any system and prepare you better for Intel Xeon Phi processors. A practical guide to the essentials for programming Intel Xeon Phi processorsDefinitive coverage of the Knights Landing architecturePresents best practices for portable, high-performance computing and a familiar and proven threads and vectors programming modelIncludes real world code examples that highlight usages of the unique aspects of this new highly parallel and high-performance computational productCovers use of MCDRAM, AVX-512, Intel(r) Omni-Path fabric, many-cores (up to 72), and many threads (4 per core)Covers software developer tools, libraries and programming modelsCovers using Knights Landing as a processor and a coprocessor"

High Performance Parallelism Pearls Volume 2 offers another set of examples that demonstrate how to leverage parallelism. Similar to Volume 1, the techniques included here explain how to use processors and coprocessors with the same programming - illustrating the most effective ways to combine Xeon Phi coprocessors with Xeon and other multicore processors. The book includes examples of successful programming efforts, drawn from across industries and domains such as biomed, genetics, finance, manufacturing, imaging, and more. Each chapter in this edited work includes detailed explanations of the programming techniques used, while showing high performance results on both Intel Xeon Phi coprocessors and multicore processors. Learn from dozens of new examples and case studies illustrating "success stories" demonstrating not just the features of Xeon-powered systems, but also how to leverage parallelism across these heterogeneous systems. Promotes write-once, run-anywhere coding, showing how to code for high performance on multicore processors and Xeon Phi Examples from multiple vertical domains illustrating real-world use of Xeon Phi coprocessors Source code available for download to facilitate further exploration

This book constitutes the proceedings of the Third Latin American Conference on High Performance Computing, CARLA 2016, held in Mexico City, Mexico, in August/September 2016. The 30 papers presented in this volume were carefully reviewed and selected from 70 submissions. They are organized in topical sections named: HPC Infrastructure and Applications; Parallel Algorithms and Applications; HPC Applications and Simulations.

Optimizing HPC Applications with Intel® Cluster Tools takes the reader on a tour of the fast-growing area of high performance computing and the optimization of hybrid programs. These programs typically combine distributed memory and

shared memory programming models and use the Message Passing Interface (MPI) and OpenMP for multi-threading to achieve the ultimate goal of high performance at low power consumption on enterprise-class workstations and compute clusters. The book focuses on optimization for clusters consisting of the Intel® Xeon processor, but the optimization methodologies also apply to the Intel® Xeon Phi™ coprocessor and heterogeneous clusters mixing both architectures. Besides the tutorial and reference content, the authors address and refute many myths and misconceptions surrounding the topic. The text is augmented and enriched by descriptions of real-life situations.

The aim of this book is to explain to high-performance computing (HPC) developers how to utilize the Intel® Xeon PhiTM series products efficiently. To that end, it introduces some computing grammar, programming technology and optimization methods for using many-integrated-core (MIC) platforms and also offers tips and tricks for actual use, based on the authors' first-hand optimization experience. The material is organized in three sections. The first section, "Basics of MIC", introduces the fundamentals of MIC architecture and programming, including the specific Intel MIC programming environment. Next, the section on "Performance Optimization" explains general MIC optimization techniques, which are then illustrated step-by-step using the classical parallel programming example of matrix multiplication. Finally, "Project development" presents a set of practical and experience-driven methods for using parallel computing in application projects, including how to determine if a serial or parallel CPU program is suitable for MIC and how to transplant a program onto MIC. This book appeals to two main audiences: First, software developers for HPC applications – it will enable them to fully exploit the MIC architecture and thus achieve the extreme performance usually required in biological genetics, medical imaging, aerospace, meteorology and other areas of HPC. Second, students and researchers engaged in parallel and high-performance computing – it will guide them on how to push the limits of system performance for HPC applications. Authors Jim Jeffers and James Reinders spent two years helping educate customers about the prototype and pre-production hardware before Intel introduced the first Intel Xeon Phi coprocessor. They have distilled their own experiences coupled with insights from many expert customers, Intel Field Engineers, Application Engineers and Technical Consulting Engineers, to create this authoritative first book on the essentials of programming for this new architecture and these new products. This book is useful even before you ever touch a system with an Intel Xeon Phi coprocessor. To ensure that your applications run at maximum efficiency, the authors emphasize key techniques for programming any modern parallel computing system whether based on Intel Xeon processors, Intel Xeon Phi coprocessors, or other high performance microprocessors. Applying these techniques will generally increase your program performance on any system, and better prepare you for Intel Xeon Phi coprocessors and the Intel MIC architecture. A practical guide to the essentials of

the Intel Xeon Phi coprocessor Presents best practices for portable, high-performance computing and a familiar and proven threaded, scalar-vector programming model Includes simple but informative code examples that explain the unique aspects of this new highly parallel and high performance computational product Covers wide vectors, many cores, many threads and high bandwidth cache/memory architecture

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